SEMESTER S8

MIXED SIGNAL CIRCUIT DESIGN

Course Code	**PEEVT 863**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	Analog VLSI design (Course code)	**Course Type**	Theory

Course Objectives:

1. To give the knowledge about various analog and digital CMOS circuits
2. To impart the skill in analysis and design of analog and digital CMOS circuits.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	CMOS Amplifiers- Common Source with diode connected loads and current source load, CS stage with source degeneration, CG stage and Source Follower (Only Voltage Gain and Output impedance of circuits) Differential Amplifiers-Differential Amplifier with MOS current source Load, with cascaded load and with current mirror load, MOS telescopic cascode amplifier. (Only Voltage Gain and Output impedance of circuits)	11
2	Band gap References- Supply Independent Biasing, Temperature independent references –band gap reference Phase Locked Loop – Simple PLL , Basic PLL Topology, Charge Pump PLL, Basic Charge Pump PLL	9
3	Dynamic analog circuits – charge injection and capacitive feed through in MOS switch, Reduction technique, Switched Capacitor Circuits- sample and hold circuits, Switched Capacitor Integrator, Ladder filters	11
4	DAC Specifications-DNL, INL, latency, SNR, Dynamic Range, DAC	9

	Architecture - Resistor String, Charge Scaling and Pipeline types. ADC Specifications-Quantization error, Aliasing, SNR, Aperture error, ADC Architecture- Flash and Pipe line types.	

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	To analyse the CMOS amplifiers and differential amplifiers	**K4**
CO2	To understand the band gap references and PLL Concepts	**K2**
CO3	To analyse the dynamic analog circuits and Switched capacitor circuits	**K4**
CO4	To understand the DAC and ADC circuits	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**	**2**									
CO2	**3**	**2**	**2**									
CO3	**3**	**3**										
CO4	**3**	**2**										**1**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	CMOS Analog Circuit Design	Phillip E. Allen, Douglas R. Holbery	Oxford	2004.
2	Fundamentals of Microelectronics	Razavi B.	Wiley student Edition	2014.

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	CMOS: Circuits Design, Layout and Simulation	Baker, Li, Boyce	Prentice Hall India	2000
2	Design of Analog CMOS Integrated Circuits	Razavi B.	Mc Graw Hill	2001

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/101/117101105/
2	https://www.youtube.com/watch?v=7xVSL93ZZq8&list=PLLDC70psjvq5vtrb0EdII4xIKA15ec-Ij&inde
3	https://www.youtube.com/watch?v=z5yaC4oEHLk
4	https://www.youtube.com/watch?v=8LuofneTOF8